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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/617,727	07/14/2003	Joon Ho Yoon	2336-193	3639

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EXAMINER	
PERKINS, PAMELA E	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/617,727	YOON, JOON HO	
	Examiner	Art Unit	
	Pamela E Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 July 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/14/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the filing of the application papers on 14 July 2003. Claims 1-11 are pending.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "3" see Figure 1; "24" see Figure 2; "32" see Figure 3(b); "56" and "57" see Figures 5(d) and 5(e). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al. (JP 06-204569) in view of Kondo et al. (JP 2000-269556).

Usui et al. disclose a method of manufacturing a light-emitting diode device where a lead frame (15) is formed including a first pattern part (13) for use in mounting a light-emitting diode (LED) chip (20) thereon, a second pattern part (12) electrically connected to the first pattern part (13) to be used as an electrode, a third pattern part (14) spaced from the first pattern part (13) to be electrically insulated from the first pattern part (13) and used as another electrode, and a fourth pattern part (16) and a fifth pattern part (16) integrated with the first pattern part (Fig. 4); plating the first, second and third pattern parts (13, 12, 14) of the lead frame (15) with a metal having high adhesion and conductivity, to prepare a plated first pattern part (13), a plated second pattern part (12), and a plated third pattern part (14); plating the fourth pattern part (16) and the fifth pattern part (16) with another metal having high reflectivity, to prepare plated fourth and fifth pattern parts (16); mounting the light-emitting diode chip (20) on the plated first pattern (13) part of the lead frame (15) (constitution); wire-bonding the light-emitting diode chip (20) mounted on the lead frame (15) to portions of the second and third pattern parts (12, 14), to form wire-bonded portions; molding (11) the light-emitting diode chip (20) and the wire-bonded portions so as to protect the light-emitting diode chip (20) and the wire-bonded portions; upwardly folding the plated fourth and fifth

pattern parts (16), neither being molded, thus forming reflective surfaces; and forming non-molded portions of the second and third pattern parts (12) to make leads (para. 9).

Usui et al. do not disclose the fourth pattern part and the fifth pattern part integrated with both sides of the first pattern part to allow surfaces of the fourth and fifth pattern parts to face each other.

Kondo et al. disclose a method of manufacturing a light-emitting diode device where a lead frame (3) is formed including a first pattern part for use in mounting a light-emitting diode (LED) chip thereon, a second pattern (3a) part electrically connected to the first pattern part to be used as an electrode, a third pattern part spaced from the first pattern part to be electrically insulated from the first pattern part and used as another electrode, and a fourth pattern part (3b) and a fifth pattern part (3b) integrated with both sides of the first pattern part (Fig. 1a); plating the first, second and third pattern parts of the lead frame (3) with a metal having high adhesion and conductivity, to prepare a plated first pattern part, a plated second pattern part (3a), and a plated third pattern part; plating the fourth pattern part (3b) and the fifth pattern part (3b) with another metal having high reflectivity, to prepare plated fourth and fifth pattern parts (3b); mounting the light-emitting diode chip on the plated first pattern part of the lead frame (3) (para. 10-16); wire-bonding the light-emitting diode chip mounted on the lead frame (3) to portions of the second and third pattern parts (3a), to form wire-bonded portions; molding (2) the light-emitting diode chip and the wire-bonded portions so as to protect the light-emitting diode chip and the wire-bonded portions; upwardly folding the plated fourth and fifth pattern parts (3b), neither being molded, to allow surfaces of the fourth and fifth pattern

parts to face each other thus forming reflective surfaces; and forming non-molded portions of the second and third pattern parts (3a) to make leads (para. 14-19).

Since Usui et al and Kondo et al. are both from the same field of endeavor, a method of manufacturing a light-emitting diode device, the purpose disclosed by Kondo et al. would have been recognized in the pertinent art of Usui et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Usui et al. by the fourth pattern part and the fifth pattern part integrated with both sides of the first pattern part to allow surfaces of the fourth and fifth pattern parts to face each other as taught by Kondo et al. to prevent breakage resulting from heat dissipation of the LED (constitution; para. 6 &7).

Referring to claim 4, Usui et al. disclose the upwardly folding step further comprises the step of controlling reflection angles of light by adjusting angles between the first pattern part and each of the fourth and fifth pattern parts (16) (Fig. 5; para. 9 & 10).

Referring to claim 5, Usui et al. disclose the molding material used at the molding step is transparent epoxy (para. 9).

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al. in view of Kondo et al. as applied to claim 1 above, and further in view of Odia et al. (6,291,274).

Usui et al. in view of Kondo et al. disclose the subject matter claimed above except plating the fourth pattern part and the fifth pattern part of the lead frame with Ag,

Ni, Pd or Cr and plating the first, second and third pattern parts of the lead frame with Ag, Au or Pd.

Odia et al. disclose a method of manufacturing a light-emitting diode device where a lead frame (20) is formed including a first pattern part (13) for use in mounting a light-emitting diode (LED) chip thereon (col. 18, lines 1-8), a second pattern (12) part electrically connected to the first pattern part to be used as an electrode; plating the first and second pattern parts (13, 12) of the lead frame (20) (col. 10, lines 18-29). Odia et al. further disclose plating the first and second pattern parts of the lead frame with Ni, Au or Pd (col. 10, lines 30-48).

Since Usui et al. and Odia et al. are both from the same field of endeavor, a method of manufacturing a light-emitting diode device, the purpose disclosed by Odia et al. would have been recognized in the pertinent art of Usui et al. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Usui et al. by plating the first and second pattern parts of the lead frame with Ni, Au or Pd as taught by Odia et al. to prevent the plated layer form peeling (col. 5, lines 46-56).

Claims 6 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al. in view of Kondo et al. and Fujiwara et al. (6,680,568).

Usui et al. in view of Kondo et al. disclose the subject matter claimed above except pre-molding the first pattern part and portions of the second and third pattern parts to be surrounded while the other portions of the second and third pattern parts are externally exposed, thus forming a package.

Fujiwara et al. disclose a method of manufacturing a light-emitting diode device where a lead frame (1) including a first pattern part (2a) for use in mounting a light-emitting diode chip (4) thereon, a second pattern part (6a) electrically connected to the first pattern part (2a) to be used as an electrode, a third pattern part (2b/6b) spaced from the first pattern part (2a) to be electrically insulated from the first pattern part (2a) and used as another electrode (Fig. 1); plating the first, second and third pattern parts (2a, 6a, 2b/6b) of the lead frame (1) with a metal having high adhesion and conductivity, prepare a plated first pattern part (2a), a plated second pattern part (6a), and a plated third pattern part (2b/6b) (col. 11, lines 21-30); pre-molding the first pattern part (2a) and portions of the second and third pattern parts (6a, 2b) to be surrounded while the other portions of the second and third pattern parts (6a, 6b)are externally exposed, thus forming a package (7); mounting the light-emitting diode chip (4) on the plated first pattern part (2a) the package (7) so that light-emitting surface of the light-emitting diode chip (4) faces upward; wire-bonding the light-emitting diode chip (4) to each of the second pattern part (6a) and the third pattern part (2b) in the package (7), to form wire-bonded portions (col. 9, lines 26-52); molding (8) the inside of the package (7) to protect the light-emitting diode chip (4) and the wire-bonded portions (Fig. 2; col. 9, lines 53-57); and forming the other portions the second and third pattern parts (6a, 6b) exposed outside the package (7) to make leads (col. 7, lines 34-42).

Since Usui et al. and Fujiwara et al. are both from the same field of endeavor, a method of manufacturing a light-emitting diode device, the purpose disclosed by Fujiwara et al. would have been recognized in the pertinent art of Usui et al. Therefore,

it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Usui et al. by pre-molding the first pattern part and portions of the second and third pattern parts to be surrounded while the other portions of the second and third pattern parts are externally exposed, thus forming a package as taught by Fujiwara et al. to increase stability (col. 3, lines 36-54).

Referring to claim 9, Usui et al. disclose the upwardly folding step further comprises the step of controlling reflection angles of light by adjusting angles between the first pattern part and each of the fourth and fifth pattern parts (16) (Fig. 5; para. 9 & 10).

Referring to claim 10, Usui et al. disclose the molding material used at the molding step is transparent epoxy (para. 9).

Referring to claim 11, Fujiwara et al. disclose the package formed at the pre-molding step is made of non-transmittable plastic materials (col. 7, lines 33-45).

Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Usui et al. in view of Kondo et al. and Fujiwara et al. as applied to claim 6 above, and further in view of Odia et al.

Usui et al. in view of Kondo et al. and Fujiwara et al. disclose the subject matter claimed above except plating the fourth pattern part and the fifth pattern part of the lead frame with Ag, Ni, Pd or Cr and plating the first, second and third pattern parts of the lead frame with Ag, Au or Pd.

Odia et al. disclose a method of manufacturing a light-emitting diode device where a lead frame (20) is formed including a first pattern part (13) for use in mounting a light-emitting diode (LED) chip thereon (col. 18, lines 1-8), a second pattern (12) part electrically connected to the first pattern part to be used as an electrode; plating the first and second pattern parts (13, 12) of the lead frame (20) (col. 10, lines 18-29). Odia et al. further disclose plating the first and second pattern parts of the lead frame with Ni, Au or Pd (col. 10, lines 30-48).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Katayama et al. (2003/0025450) disclose plating the first and second pattern parts of the lead frame with Ni, Au or Pd.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PEP

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